

## CLAIMS:

1. A ferroelectric device (10) with a body (11) comprising a substrate (1) and a ferroelectric layer (2) provided with a connection conductor (3) on a side facing away from the substrate (1), which ferroelectric layer contains an oxygen-free ferroelectric material and is used to form an active electrical element (4), characterized in that a conductive layer (5) is  
5 situated between the substrate (1) and the ferroelectric layer (2), which conductive layer forms a further connection conductor (5) of the ferroelectric layer (2), and the active electrical element (4) is formed as a result of the fact that the ferroelectric layer (2) forms a Schottky junction with at least one of the connection conductors (3, 5).
- 10 2. A ferroelectric device (10) as claimed in claim 1, characterized in that the active electrical element (4) is a memory element (4).
3. A ferroelectric device (10) as claimed in claim 2, characterized in that the  
body (11) comprises a semiconductor body (11), and the substrate (1) comprises a, preferably  
15 monocrystalline, semiconductor substrate (1).
4. A ferroelectric device (10) as claimed in claim 3, characterized in that the  
semiconductor body (11) comprises a field effect transistor (6) with a source region (7), a  
drain region (8) and a gate electrode (9), and the further connection conductor (5) is situated  
20 on the source or drain region (7) of the field effect transistor and also serves as a connection  
conductor (5) of the source region or drain region (8).
5. A ferroelectric device (10) as claimed in claim 4, characterized in that the  
memory element (4) and the source or drain region (7) show an overlap, viewed in  
25 projection.
6. A ferroelectric device (10) as claimed in claim 4 or 5, characterized in that the  
Schottky junction is formed between the further connection conductor (5) and the  
ferroelectric layer (2), and the further connection conductor (5) forms an ohmic contact with

the source or drain region (7) of the field effect transistor (6), while the connection conductor (3) forms an ohmic contact with the ferroelectric layer (2).

7. A ferroelectric device (10) as claimed in any one of the preceding claims,  
5 characterized in that a chalcogenide is selected as the ferroelectric material.

8. A ferroelectric device (10) as claimed in claim 7, characterized in that the  
selected chalcogenide is  $Zn_xCd_{1-x}S$ , preferably  $Zn_xCd_{1-x}S$  having a Zn content of x in the  
range between 0.3 and 0.5.

10 9. A ferroelectric device (10) as claimed in claim 8, characterized in that Pt or Au  
is selected as the material for one connection conductor (3) and Ag or Al is selected as the  
material for the other connection conductor (5).

15 10. A ferroelectric device (10) as claimed in claim 7, characterized in that  $Cu_2S$  is  
selected as the chalcogenide.

11. A ferroelectric device (10) as claimed in claim 10, characterized in that Cu is  
selected as the material for one connection conductor (3) and W is selected as the material for  
20 the other connection conductor (5).

12. A ferroelectric device (10) as claimed in claim 2, 3, 4, 5 or 6, characterized in  
that the doping concentration of the oxygen-free ferroelectric material is so high that an  
ohmic contact between the connection conductor (3) or the further connection conductor (5)  
25 and the ferroelectric layer (2) is formed, and that, during operation, the electric field in the  
ferroelectric layer (2) in the conducting state is sufficiently high to switch off the memory  
element (4).

13. A ferroelectric device (10) as claimed in Claim 12, characterized in that said  
30 ferroelectric device comprises a matrix of N x M memory elements (4), where N and M are  
natural numbers and each memory element (4) is connected on both sides to an electric  
connection (20, 30).

14. A ferroelectric device (10) as claimed in claim 13, characterized in that each memory element (4) is coupled to an associated field effect transistor (6) with a source region (7), a drain region (8) and a gate electrode (9), and the device is provided with N first conductor tracks (20), M second conductor tracks (30) and with a ground connection (40), and each memory element (4) is connected via the connection conductor (3) to one of the N first conductor tracks and via the further connection conductor (5) to the source or drain region (7) of the field effect transistor (6), of which the other drain or source region (8) is connected to the ground connection (40), while the gate electrode (9) of the field effect transistor (6) is connected to one of the M second conductor tracks (30).

15. A ferroelectric device (10) as claimed in claim 1, characterized in that the active electrical element (4) is a diode.

16. A method of manufacturing a ferroelectric device (10) as claimed in any one of the preceding claims, wherein a body (11) is formed that comprises a substrate (1), and the device (10) is provided with a ferroelectric layer (2) provided with a connection conductor (3) on a side facing away from the substrate (1), an oxygen-free ferroelectric material being selected as the material for the ferroelectric layer which is used to form an active electrical element (4), characterized in that a conductive layer is provided between the substrate (1) and the ferroelectric layer (2), which conductive layer forms a further connection conductor of the ferroelectric layer (2), and the memory element (4) is obtained by forming a Schottky junction between the ferroelectric layer (2) and at least one of the connection conductors (3, 5).

17. A method according to claim 16, characterized in that the active electrical element (4) is formed as a memory element (4).

18. A method as claimed in claim 17, characterized in that the body (11) is formed so as to be a semiconductor body (11), and a semiconductor substrate (1) is selected as the substrate (1).

19. A method as claimed in claim 17, characterized in that in the semiconductor body (11) there is formed a field effect transistor (6) with a source region (7), a drain region (8) and a gate electrode (9), and the further connection conductor (5) is provided on the

source or drain region (7) of the field effect transistor (6) and is formed so as to be a connection conductor (5) of the source region or drain region (7).

20. A method as claimed in claim 17, 18 or 19, characterized in that the Schottky  
5 junction is formed between the further connection conductor (5) and the ferroelectric layer (2), and an ohmic contact is formed between the connection conductor (3) and the ferroelectric layer (2) as well as between the further connection conductor (5) and the source or drain region (7) of the field effect transistor (6).

10 21. A method as claimed in claim 17, 18, 19 or 20, characterized in that the ferroelectric layer (2) is formed by converting part of a conductive layer to the ferroelectric material, one of the connection conductors (3, 5) being formed by the remaining part of the conductive layer.

15 22. A method as claimed in any one of claims 17 through 21, characterized in that a matrix of  $N \times M$  memory elements (4) is formed, where  $N$  and  $M$  are natural numbers and each memory element (4) is provided on both sides with an electric connection.

23. A method as claimed in claim 22, characterized in that each memory element  
20 (4) is coupled to a field effect transistor (6) formed in the device (10) and associated with said memory element (4), which field effect transistor comprises a source region (7), a drain region (8) and a gate electrode (9), and the device (10) is provided with  $N$  first conductor tracks (20),  $M$  second conductor tracks (30) and with a ground connection (40), and each memory element (4) is connected via the connection conductor (3) to one of the  $N$  first  
25 conductor tracks (20) and via the further connection conductor (5) to the source or drain region (7) of the associated field effect transistor (6), of which the other drain or source region (8) is connected to the ground connection (40), while the gate electrode (9) is connected to one of the  $M$  second conductor tracks (30).

30 24. Method of operating a ferroelectric device (10) as claimed in claim 15, characterized in that the ferroelectric device (10) is operated outside the voltage region where the ferroelectric memory effect occurs.